Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.040”**

**.040”**

**12 11 10**

**9**

**8**

**7**

**13**

**14**

**1**

**2**

**3 4 5 6**

**S00C**

**MASK**

**REF**

**PAD FUNCTIONS:**

1. **1A**
2. **1B**
3. **1Y**
4. **2A**
5. **2B**
6. **2Y**
7. **GND**
8. **3Y**
9. **3A**
10. **3B**
11. **4Y**
12. **4A**
13. **4B**
14. **VCC**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: S00C**

**APPROVED BY: DK DIE SIZE .040” X .040” DATE: 8/18/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .014” P/N: 54S00**

**DG 10.1.2**

#### Rev B, 7/1